Magnetic random access memory and fabricating method thereof

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Abstract of **TW 466486 (B)**

An improved and novel MRAM device with magnetic memory elements and circuitry for controlling magnetic memory elements is provided. The circuitry, for example, transistor (12a) having a gate (17a), a drain (18) and a source (16a) is integrated on a substrate (11) and coupled to a magnetic memory element (43) on the circuitry through a plug conductor (19a) and a conductor line (45). The circuitry is fabricated first under the CMOS process and then magnetic memory elements (43, 44). Digit line (29) and bit line (48) are placed under and on top of magnetic memory element (43), respectively, and enabled to access magnetic memory element (43). These lines are enclosed by a high permeability layer (31, 56, 58) excluding a surface facing magnetic memory element (43), which shields and focuses a magnetic field toward magnetic memory element (43).